

# PATENT ABSTRACTS OF JAPAN

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(71)Applicant : NEC CORP

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## (54) SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

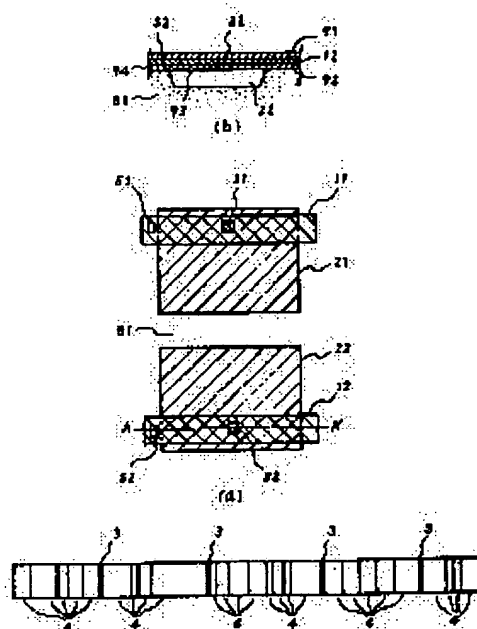
### (57)Abstract:

**PURPOSE:** To reduce an impedance of power supply line in the vicinity of the center of logic cell columns and to prevent drop of signal transfer speed by forming a capacitance within power feeding cells and by arranging power feeding cells in the logic cell columns with an adequate space.

**CONSTITUTION:** A power feeding cell is formed with power feeding lines 11, 12 where the power feeding lines of a first wiring layer are arranged with the same interval, a P type diffusion region 21, an N type diffusion region 22, a first wiring layer-diffusion contacts 31, 32, substrate-first wiring layer contacts 51, 52 and insulating films 91~94.

In this power feeding cell, a junction capacitance is formed between the P type diffusion region 21 and substrate 81. In addition, since the power feeding lines 11, 12 and diffusion regions 21, 22 are connected with the first wiring layer-diffusion contacts 31, 32, a junction

capacitance is formed between the power feeding lines 11, 12. Here, when such power feeding cells 3 are arranged with an adequate interval between the logic cells 4, dispersion of potential of power feeding line can be reduced and drop of signal transfer speed can be prevented.



## LEGAL STATUS

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